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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/362,504	07/27/1999	KRAMADHATI V. RAVI	AM1126D1/T08	6922

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EXAMINER	
ZERVIGON, RUDY	
ART UNIT	**PAPER NUMBER**
1763	

24

DATE MAILED: 10/22/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/362,504	RAVI ET AL.	
	Examiner	Art Unit	
	Rudy Zervigon	1763	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

P riod for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 September 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *16-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *16-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

2. Claim 16 is rejected under 35 U.S.C. 102(b) as being anticipated by Jin Onuki et al. Jin Onuki et al have described improvements in integrated circuit step coverage and electromigration resistance of aluminum films when employing switching bias sputtering power (abstract, right column, mid second, last paragraphs page 182). The switching bias sputtering power described by Jin Onuki et al are embodied as "two-step bias application" (right column, last paragraph page 182). The two-step bias application is further described by Jin Onuki et al according to a method ordered according to "a deep d.c. bias of -200V, and, second, a shallow d.c. bias of 50V for 10s" (section 2.1 - Film Formation). The method of the Jin Onuki et al process is embodied in repetitive cycles as shown in Figure 1(b).

Implicit in the cyclic application of the two-step switching bias sputtering power method described by Jin Onuki et al and, according to the step waveforms shown in Figure 1(b), is an unbiased time frame, in each cycle, prior to the application of the first "deep d.c. bias of -200V". It is entrusted that the establishment of a gas in a plasma state necessarily requires "flowing a process gas into a substrate processing chamber" and "forming a plasma from said process gas" by "coupling energy into said substrate processing chamber". Figure 1b shows switching cycles each of which have zero biasing voltage time frames (abscissa) prior to application of -200V for 5, 30, or 90 seconds. Jin Onuki also provides teaching of maintaining the application of the

sputtering power to the reactants while biasing the plasma towards the substrate according to figure 1a page 183.

Jin Onuki also teaches applying silicon and oxygen process gasses for film deposition ("0.5μm thermally grown SiO_2 layer", section 2.1).

Claim Rejections - 35 USC § 103

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. Claims 17, 18, 25-28, and 32-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ye et al (U.S. Pat. 5,710,486) in view of Jin Onuki et al, Boys et al (U.S.Pat. 4,500,408), Ramarotafika et al.

Ye et al describe an "inductively and multi-capacitively coupled plasma reactor" (Title) for substrate processing comprising:

i. A housing for forming a vacuum chamber (items 52/54, Figure 3, column 3, lines 49-51)

ii. A vacuum pump for forming evacuating the vacuum chamber (implied)

iii. A pedestal (item 60, Figure 3, column 3, lines 52-53), located within the housing for forming a vacuum chamber (items 52/54, Figure 3, column 3, lines 49-51), configured to hold a substrate (item 61, Figure 3, column 3, line 52-53)

iv. A gas distribution system fluidly coupled to the vacuum chamber (column 3, lines 12-16)

v. A plasma generation system (column 3, lines 62-67) for forming a plasma from a process gas within housing for forming a vacuum chamber (items 52/54, Figure 3, column 3, lines 49-51)

vi. RF energy (78, Figure 3) applied to a coil (74, Figure 3) disposed about the processing chamber (52, Figure 3)

vii. Electrical energy is applied to the first (62, Figure 3) and second (60, Figure 3) electrodes while maintaining the application of RF energy (72, Figure 3)

viii. Ye et al additionally teaches the establishment of a gas in a plasma state by "flowing a process gas into a substrate processing chamber" and "forming a plasma from said process gas" by coupling and maintaining energy into said substrate processing chamber.

ix. Selective biasing of the generated plasma towards the processing substrate is provided according to the independently powered capacitive electrode (item 60, Figure 5) that supports the substrate (Figure 5; column 3, lines 49-67)

x. A controller (implied according to column 2, lines 56-59) for controlling plasma generation means

Ye et al do not teach a controller (implied according to column 2, lines 56-59) for controlling a vacuum pump and a gas distribution system. And so Ye et al would be modified by adding a controller as taught by Jin Onuki et al.

Jin Onuki et al introduce improvements in integrated circuit step coverage and electromigration resistance of aluminum films when employing switching bias sputtering power (abstract, right column, mid second, last paragraphs page 182). The switching bias sputtering power described by Jin Onuki et al are embodied as "two-step bias application" (right column, last paragraph page 182). The two-step bias application is further described by Jin Onuki et al according to a method ordered according to "a deep d.c. bias of -200V, and, second, a shallow d.c. bias of 50V for 10s" (section 2.1 - Film Formation). The method of the Jin Onuki et al process is embodied in

repetitive cycles as shown in Figure 1(b). Implicit in the cyclic application of the two-step switching bias sputtering power method described by Jin Onuki et al and, according to the step waveforms shown in Figure 1(b), is an unbiased time frame, in each cycle, prior to the application of the first "deep d.c. bias of -200V". Thus the Jin Onuki et al reference describe a method of deposition wherein there is selective electrode biasing to deposit a first layer without biasing the generated plasma towards the substrate, and subsequent second layer deposition under biased conditions: "a deep d.c. bias of -200V, and, second, a shallow d.c. bias of 50V for 10s" (section 2.1 - Film Formation). As discussed above, implicit in the cyclic application of the two-step switching bias sputtering power method described by Jin Onuki et al and, according to the step waveforms shown in Figure 1(b), is an unbiased time frame, in each cycle, prior to the application of the first "deep d.c. bias of -200V". Successive cycles, as shown in Figure 1(b), provide additional deposited layers. Ye et al and Jin Onuki et al do not explicitly describe programmable memory controller for controlling the process vacuum pump, gas distribution system.

Boys et al teaches a programmable memory controller for controlling the process vacuum pump, gas distribution system, and plasma generation means. Boys et al further describe a magnetron sputter coating apparatus controlled in response to measurements of plasma parameters to control deposition parameters (abstract). Specifically, Boys et al describe a CPU *computer* 57 which includes a conventional memory for storing a program and predetermined data for controlling the operation of sources 25 and 37, as well as orifice 32. The programmed values for the voltage and current of source 37 and the *pressure* in volume 13 are stored in the memory of CPU 57.

Additionally, vacuum pump control is discussed according to adding another "variable pumping orifice" (column 8, lines 8-13; column 7, lines 38-40).

Ramarotafika et al describe the influence of d.c. bias (including unbiased states) of WTi films (section 3).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the control systems, as described by Boys et al, in the Ye et al apparatus consistent with a deposition method as promoted by Jin Onuki et al and Ramarotafika et al.

Motivation for combining the above references follows from the desire to control plasma process attributes as discussed by the Boys et al (column 3, lines 25-67) with a deposition method of Jin Onuki et al supporting motivation directed to "high-quality films"(abstract, right column, mid second, last paragraphs page 182).

1. Claims 19-24, 29-31, 35, and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ye et al (U.S. Pat. 5,710,486) in view of Jin Onuki et al, Boys et al (U.S.Pat. 4,500,408), Ramarotafika et al, as applied to claims 17, 18, 25-28, and 32-34 above, and further in view of Matsuura (U.S.Pat. 5,319,247). Jin Onuki et al describes switching bias sputtering power application embodied as "two-step bias application" (right column, last paragraph page 182). Matsuura describes a method of forming silicon and oxygen combined thin films for "superior crack resistance and insulation" (silicate, column 6, lines 4-11) by optionally (embodiment) applying silane and oxygen gases (column 7, line 67; claim 1). Operating conditions of pressure: 1mTorr≤100mT≤10Torr (column 6, line 33) and temperature: 100°C≤350°C≤450°C≤500°C (column 6, line 38) are specifically met by Matsuura.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to consider application of the Matsuura method, in the Ye et al apparatus, for forming silicon and oxygen combined thin films for "superior crack resistance and insulation" (silicate, column 6, lines 4-11) by optionally (embodiment) applying silane and oxygen gases (column 7, line 67; claim 1).

Motivation for combining the above references follows from the Matsuura identified improved substrate rigidity, or reducing mechanical stress, and electrical isolation as for "superior crack resistance and insulation" (silicate, column 6, lines 4-11).

Conclusion

1. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Rudy Zervigon whose telephone number is (703) 305-1351. The examiner can normally be reached on a Monday through Thursday schedule from 8am through 7pm. The official after final fax phone number for the 1763 art unit is (703) 872-9311. The official before final fax phone number for the 1763 art unit is (703) 872-9310. Any Inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Chemical and Materials Engineering art unit receptionist at (703) 308-0661. If the examiner can not be reached please contact the examiner's supervisor, Gregory L. Mills, at (703) 308-1633.